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Title :SAME CHANNEL FREQUENCY INTERFERENCE REDUCING CIRCUIT AND TELEVISION BROADCASTING RECEIVER

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SAME CHANNEL FREQUENCY INTERFERENCE REDUCING CIRCUIT AND TELEVISION BROADCASTING RECEIVER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an interference reducing circuit for reducing an interference wave that is mixed in a reception wave. In particular, the invention relates to a TV broadcasting receiver that is equipped with an interference reducing device that effectively reduces an interference wave or the like that will act as a disturbance wave to a broadcast signal received by a digital broadcasting receiver and that is suitable for use in a receiving apparatus.

2. Description of the Related Art

As opposed to conventional analog transmission type TV broadcasts, digital multi-channel broadcasts using a satellite have already been realized though they are commercial ones. To effectively utilize the transmission bands, it is desired that digital versions (hereinafter referred to as "digital broadcasts") of ground-wave broadcasts be realized and spread.

However, conventional ground-wave analog broadcasts (hereinafter referred to as "analog broadcasts") will not be switched to digital broadcasts all at once and the two kinds of broadcasting will coexist in the initial stage of the transition. For example, since it is planned to send digital broadcasts using

part of the current UHF broadcasting channels, unused channels of each area can be used for digital TV broadcasts or digital radio broadcasts.

The OFDM (orthogonal frequency division multiplexing) scheme in which data is transmitted being distributed to many carriers is employed for transmission of a broadcast wave of a digital TV broadcast. The OFDM is a transmission scheme in which ghosts do not tend to occur because signal processing can be performed so that one data symbol lasts for a long time.

Being a modulation scheme in which ghosts do not tend to occur, the OFDM has an advantage that it can be used for an SFN (single frequency network) in which relay broadcasting stations that relay the same program can use the same transmission frequency. Further, even if a particular carrier is affected by selective fading, only part of data is lost and error correction is enabled.

In the NTSC broadcasting area, a plan is such that the broadcasting bandwidth of each broadcasting channel will be made 6 MHz as in the case of the analog broadcasting. In the OFDM scheme, since digitized video/audio information is sent simultaneously by using thousands of carrier waves, sending power that is modulated by a digital signal and then output is distributed to many, approximately uniform spectral components in a certain broadcasting channel (6 MHz) as indicated by "OFDM" in Fig. 7. In contrast, like a spectrum shown in the lower part of Fig. 7, the power of an analog broadcast in the same channel is such

that a video carrier Pv that is amplitude-modulated according to video information and an audio subcarrier Pa that is frequency-modulated according to an audio signal give peak levels and broadcast power spectral components are distributed around the carriers Pv and Pa. In particular, the peak levels of the carriers Pv and Pa are prominent.

Therefore, when in the future a channel in the UHF band is assigned to a digital broadcast, if the same channel close to it is used for an analog broadcast, the video carrier Pv and the audio subcarrier Pa of the analog broadcast may act as strong interference waves to the digital broadcast as seen from Fig. 7. Even if the same channel is not used for an analog broadcast, there is fear that particularly the audio subcarrier component Pa' of an adjacent analog broadcast channel will leak into the digital broadcast channel due to a multi-path or fading phenomenon and cause interference as shown in Fig. 8 depending on the frequency selection characteristic of a high-frequency circuit. Depending on the IF characteristic of a receiver, the interference wave component may be demodulated as digital data to increase the error rate of demodulated data and cause picture disappearance or image quality deterioration. For a similar reason, the video carrier Pv' of a channel that is adjacent to and higher than the reception channel may act as an interference wave.

In view of the above, it was proposed to reduce interference by inserting a comb filter, a notch filter, or the like that

is designed in consideration of an interference wave in an RF circuit of a receiving section, to thereby cancel a carrier component of another station that will act as an interference wave to a digital broadcasting channel (Japanese Patent Application No. Hei. 10-11018). However, since general band-pass filters have a comb-shaped attenuation characteristic, the reduction of an interference wave in the same channel causes reduction of digital data. For this reason, this measure cannot increase the error correction rate of demodulated data to a large extent. In particular, it is difficult to eliminate a lower adjacent audio signal of a channel adjacent to the reception channel. There is a problem that to attain, by means of a filter or the like, reduction at an interference frequency where an interference wave may occur, interference waves cannot be reduced in a stable manner because the reduction frequency shifts from the target frequency due to a drift of a local frequency of a receiver.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above circumstances in the art, and an object of the invention is therefore to enable reduction of an interference wave by providing a phase locking means for attaining phase locking to a wave that will interfere with a receiver and a level adjusting means capable of adjusting the level of a phase-locked signal produced by the

phase locking means, generating a replica of a main interference wave frequency signal by means of the phase locking means and the level adjusting means, and subtracting the interference wave frequency signal from a reception signal.

According to a first aspect of the invention, there is provided an interference reducing circuit comprising phase locking means for attaining phase locking to an interference wave having a carrier frequency that is received together with a reception wave by tuning; level adjusting means for adjusting a level of a phase-locked signal that is output from the phase locking means; and subtracting means for subtracting the level-adjusted, phase-locked signal from the reception wave. The reception wave from which the interference wave signal component is eliminated is output from the subtracting means.

According to a second aspect of the invention, the phase locking means comprises a voltage-controlled oscillator for producing a signal having a frequency that is varied by voltage control; phase comparing means for comparing phases of an output of the voltage-controlled oscillator and the interference wave; and a feedback circuit for feeding back, as a control voltage for the voltage-controlled oscillator, via a second-order loop filter, a phase error signal that is produced by the phase comparing means.

According to a third aspect of the invention, the level adjusting means comprises a first-order loop filter and adjusts

a level of the interference wave based on a level of a signal produced by the phase locking means.

According to a fourth aspect of the invention, the interference wave is an amplitude-modulated or frequency-modulated carrier, and wherein a loop characteristic of the phase locking means is so set as to follow an amplitude modulation component or a frequency modulation component. This makes it possible to reduce an interference wave signal even if it is an AM or FM carrier.

According to a fifth aspect of the invention, there is provided a TV receiver comprising receiving means for receiving a transmitted broadcast including video or audio information; an A/D converter for converting, into digital information, a video or audio signal received by the receiving means; a signal processing circuit for demodulating the digital information of the video or audio information that is output from the A/D converter; phase locking means for attaining phase locking to interference wave information that is mixed in the digital information that is output from the A/D converter; level adjusting means for adjusting a level of the interference wave information to which phase locking is attained by the phase locking means; and subtracting means for subtracting the level of the interference wave information obtained by the level adjusting means from the video or audio information.

According to a sixth aspect of the invention, the phase

locking means attains locking to an interference wave frequency signal that is video carrier information or audio subcarrier information of another analog TV reception wave that is set in the same channel as the broadcast.

According to a seventh aspect of the invention, the phase locking means comprises a sinusoidal information signal generating section for producing a signal having a phase that is varied in accordance with control information; phase comparing means for comparing phases of an output of the sinusoidal information signal generating section and the interference wave; and a feedback circuit for feeding back, as a control voltage for the sinusoidal information signal generating section, via a second-order loop filter, a phase error signal that is produced by the phase comparing means.

According to an eighth aspect of the invention, the level adjusting means comprises a first-order loop filter and adjusts the level of the interference wave based on a level of a signal produced by the subtracting means.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a basic block diagram of an interference reducing device;

Figs. 2A-2C show how an interference signal is reduced;

Fig. 3 is a block diagram of a TV broadcasting receiver having an interference reducing circuit according to the

invention;

Fig. 4 is a block diagram of another TV broadcasting receiver having an interference reducing circuit according to the invention;

Fig. 5 is a block diagram of a phase locking section that is part of an interference reducing circuit;

Fig. 6 is a block diagram of a level adjusting section for adjusting the level of an extracted interference wave signal;

Fig. 7 shows a spectrum of a digital broadcast reception wave and an interference wave signals; and

Fig. 8 shows interference waves that are mixed into a digital broadcast reception wave from an adjacent channel.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figs. 1 and 2A-2C outline an interference reducing device of a receiver according to the present invention.

In Fig. 1, reference numeral 1 denotes an antenna for receiving radio waves Pa and numeral 2 denotes a receiving section for tuning in to a desired channel of the received radio waves Pa. It is assumed that the antenna 1 simultaneously receives a radio wave Pi that will act as a disturbance wave and the receiving section 2 performs first demodulation on it. Reference numeral 3 denotes a phase locking circuit provided on the output side of the receiving section 2. For example, the phase locking circuit 2 is a PLL circuit that attains phase locking particularly at

the frequency of an interference wave among input signals.

Reference numeral 4 denotes a level adjusting circuit for adjusting the signal level of a phase-locked signal that is output from the phase locking circuit 3. An adjusted signal that is output from the level adjusting circuit 4 is supplied to a subtracter 5 as a replica of an interference wave signal.

The subtracter 5 is also supplied with a reception signal that is received by the receiving section 2. The subtracter 5 eliminates that component of the reception signal which has the frequency of the replica of the interference wave signal.

The reception signal from which the component having the frequency of the replica of the interference wave signal is eliminated is fed back to the level adjusting circuit 4, whereby the level of the replica of the interference wave signal is adjusted.

How an interference wave is reduced will be described below by using signal spectra (envelopes) of reception radio waves shown in Figs. 2A-2C. It is assumed that as shown in Fig. 2A a spectrum Si of a radio wave that will act as an interference wave having a very high peak level is mixed in a frequency spectrum Sa (bandwidth: BW) of a channel that is received by the antenna 1 and selected by the receiving section 2.

Usually, the PLL circuit as the phase locking circuit 3 has a locking range and a capturing range having prescribed values. Therefore, if the PLL circuit is so configured that its vicinity

of the frequency of the spectrum Si of a radio wave that will act as an interference wave is included in the locking range and the other frequency portions are out of the capturing range, as shown in Fig. 2B the PLL circuit attains phase locking at the frequency of the interference wave spectrum having the highest level in the locking range and produces a PLL output signal S_{PLL}.

The PLL output signal S_{PLL} is supplied to the level adjusting circuit 4, which performs control so that the level of the PLL output signal S_{PLL} becomes equal to the signal level of the interference wave frequency spectrum Si of the spectrum of the received radio waves. Therefore, the level adjusting circuit 4 outputs a signal that is a replica of the interference wave signal that is mixed in the reception signal in the selection range of the receiving section 2. By subtracting the replica of the interference wave signal from the output signal of the receiving section 2, a signal having a spectrum envelope Pa' shown in Fig. 2C is obtained in which the interference wave spectrum Si having different information than information in the reception channel is eliminated.

If a signal that will act as an interference wave is modulated according to information, the spectrum Si of the signal has a prescribed bandwidth with its frequency or amplitude varied. The device can follow a frequency variation of an interference wave by properly setting the loop time constant of the PLL circuit and can also follow an amplitude variation by properly setting

the control loop time constant of the level adjusting circuit 4.

Fig. 3 is a block diagram showing an embodiment in which the above-described interference reducing circuit is applied to a TV broadcasting receiver. In Fig. 3, reference numeral 1 denotes an antenna for receiving digital broadcasts. Reference numeral 6 denotes a tuner section for tuning in to a desired channel. Reference numeral 7 denotes a digital signal processing section for demodulating an output of the tuner section 6 into digital data through conversion into an IF frequency and decoding it into a broadcasting-station-side database signal through various kinds of signal conversion.

A digital signal that is output from the digital signal processing section 7 is supplied to a phase locking circuit 8 and a level adjusting circuit 9 that constitute an interference reducing circuit according to the invention. Information included in an interference wave signal is detected by the circuits 8 and 9 and supplied to a digital signal processing circuit 10.

The phase locking circuit 8 is a PLL (hereinafter referred to as DPLL) circuit that is a digital circuit. The phase locking circuit 8 may be a digital signal processing type PLL circuit using various digital operation elements that perform operations on digital data itself without converting it into a digital signal waveform.

As the digital signal processing circuit 10, a DSP (digital

signal processor) that performs various kinds of digital signal processing is used in accordance with the contents of a modulation wave. For example, where transmission data is formed by video information, a signal that is coded according to the MPEG2 is input to a dedicated DSP that produces time-axis video data by performing DCT (discrete cosine transform) and motion compensation inter-frame predictive decoding, forms frame image data, and expands compressed video information.

Where transmission data is audio information, different kinds of signal processing are performed depending on whether the information is of a monaural broadcast or a stereo broadcast. In the case of a multi-channel broadcast wave obtained by modulating stereo signals or digital data according to a special modulation method, compressed data is also converted into the original audio information by a dedicated DSP. Such digital signal processing is already employed commonly in receivers for receiving satellite broadcast waves, and hence it is not described here in detail.

Operating in the same manner as the phase locking circuit 3 and the level adjusting circuit 4 shown in Fig. 1, the phase locking circuit 8 and the level adjusting circuit 9 that is a digital circuit cancel data information that is mixed as an interference wave in digital information data obtained by demodulating a reception signal.

The receiver as shown in Fig. 3 operates properly in

receiving a desired signal according to the OFDM scheme. There is possibility that in the future such a receiver will be used for reception of radio broadcasts and FM broadcasts. In such a case, various kinds of information as data are superimposed on audio information and received. In digital receivers, the error correction rate of data decreases if a carrier of another broadcast frequency that will act as a disturbance wave is mixed in a desired reception channel. However, in the case of the embodiment of the invention, since the above-described interference reducing device for processing reception information that is converted into a digital signal is added in the form of the phase locking circuit 8 and the level adjusting circuit 9, the SNR can be increased.

As described above, the phase locking circuit 8 generates a signal component that is phase-locked to an interference wave in a reception channel. This signal component is supplied to the level adjusting circuit 9 that performs control so that the level of the signal component becomes equal to the level of the signal that is received as the interference wave. A replica of the interference wave signal that is output from the level adjusting circuit 9 is used in the digital signal processing circuit 10 to eliminate the interference wave from demodulation data.

The DPLL circuit as the phase locking circuit 8 prohibits the interference wave compensation operation if the level and

the frequency of an input signal are not within certain ranges, that is, if the level of a signal that will act as an interference wave is equivalent to or smaller than the signal level of a desired wave. That is, the interference reducing circuit is so configured as to output an interference signal component particularly when the desired reception wave is a digitally modulated signal and a signal that will act as an interference wave is received as an analog signal obtained by modulating a single carrier and having a level that is higher than or equal to a certain level.

Where the frequency of an interference wave is known in advance, by setting the fundamental frequency of the DPLL circuit as the phase locking circuit 8 in the vicinity of the interference wave frequency and making the locking range narrow, the interference reducing circuit can be applied to a receiver that receives transmission radio waves according to any of various schemes obtained by digitally modulating a single carrier according to a multi-value signal rather than OFDM radio waves.

Fig. 4 shows an embodiment in which the interference reducing circuit according to the invention is applied to a digital TV receiver. In Fig. 4, reference character A denotes an antenna for receiving a digital broadcast, numeral 11 denotes a front tuner, and numeral 12 denotes an amplifier for amplifying an IF signal. The amplifier 12 may be omitted depending on the front tuner 11. Reference numeral 13 denotes an A/D conversion section for converting an IF signal into a digital signal. The sampling

frequency of the A/D conversion section 13 is so set as to allow the A/D conversion section 13 to output a quantized signal (e.g., complex data) that is digital data of 10 bits, for example, generated by using a clock signal that satisfies at least the Nyquist condition. Ideally, it is preferable that the sampling frequency be two or more times the IF frequency. However, for interference reduction, the sampling may be performed at a sampling period t_{sam} (= 0.5) that is approximately a half of the signal rate period t_{sym} (= 1) of a reception signal.

Reference numeral 14 denotes a first interference reducing circuit section for detecting, as an interference wave, a video carrier of another analog TV channel signal that is mixed in a selected channel. The first interference reducing circuit section 14 consists of a phase locking section 14a and a level adjusting section 14b as described above. Reference numeral 15 denotes a second interference reducing circuit section for eliminating, as an interference wave, an audio subcarrier of another analog TV channel signal that is mixed in a reception channel. The second interference reducing circuit section 15 likewise consists of a second phase locking section 15a and a level adjusting section 15b.

The first phase locking section 14a is a DPLL circuit that captures reception digital data that is output from the A/D conversion section 13 and outputs a signal that is synchronized with a video carrier that will act as an interference wave. The

first phase locking section 14a outputs a synchronized signal PLL1 and its conjugate signal CPL1. The first level adjusting section 14b receives, as inputs In2 and In3, the outputs PLL1 and CPL1 of the first phase locking section 14a, and produces an output Lv1 that is digital data obtained by adjusting, based on reception digital data as an input In1, a phase-locked interference wave signal so that its level becomes equal to a level corresponding to a reception video carrier signal as well as an output CompLv1 that is digital data obtained by eliminating data of the interference wave from the reception data.

Therefore, the first level adjusting section 14b produces, as the output Lv1, a replica of the carrier component of the analog video signal that is mixed in the same channel and also produces, as the output CompLv1 of the first level adjusting circuit, a signal in which the interference wave component whose replica is output as the output Lv1 is eliminated. The output CompLv1 is input to the second phase locking section 15a that is the DPLL circuit and the second level adjusting section 15b.

The second phase locking section 15a, which is configured in the same manner as the first phase locking section 14a, is so set as to attain phase locking to an audio subcarrier that is mixed as an interference wave. The second phase locking section 15a supplies the second level adjusting section 15b with outputs PLL2 and CPL2 that are digital data of the audio subcarrier to which phase locking is made as an interference wave. The output

CPL2 is a conjugate signal of the output PLL2. The second level adjusting section 15b receives, as inputs In2 and In3, the outputs PLL2 and CPL2 of the second phase locking section 15a, and produces an output Lv2 that is digital data obtained by adjusting, based on the output CompLv1 as an input In1, a phase-locked interference wave signal so that its level becomes equal to a level corresponding to a reception audio subcarrier signal as well as an output CompLv2 that is digital data obtained by eliminating data of the interference wave from the reception data.

The level-adjusted output Lv2 of the second level adjusting section 15b is added to the output Lv1 of the first level adjusting section 14b by an adder (subtracter) 16, whereby a replica signal of the interference wave resulting from the analog TV signal that is mixed in the reception channel is output.

A signal obtained by eliminating the replica signal of the interference wave from the reception digital TV information, that is, the digital data CompLv2 of the reception wave that has been compensated for the interference component, is output from the second level adjusting section 15b and supplied to a digital signal processing section 17 as in the above-described case. In the digital signal processing section 17, video information and audio information are restored by decoding. The video information is subjected to various kinds of digital decoding processing and a component video signal is finally supplied to a display means.

For example, where transmission data is formed by video information, a spectrum of each carrier is obtained through Fourier transform and data of each carrier is P/S-converted into demodulation data. Since the demodulation data is such that the video information is compressed according to the MPEG2, for example, the demodulation data is input to a DSP that is dedicated to expansion of such data. The audio information is separated from the video information. Data of separated digital audio information is decoded into original digital audio data, based on which an analog audio signal is formed. In this manner, the digital signal processing section 17 restores video component data and audio data through decoding and outputs a composite video signal and an audio signal to a TV receiver in the same manner as in set-top boxes for digital television that are already put to practical use.

Fig. 5 is a block diagram showing a specific example of the first phase locking section 14a or the second phase locking section 15a that is used in the TV receiver of Fig. 4. The pull-in operations performed by the first phase locking section 14a and the second phase locking section 15a are essentially the same, though they are different from each other in detail depending on whether the interference wave to which the DPLL circuit attains locking is a video carrier or an audio subcarrier.

In Fig. 5, reference numeral 21 denotes a multiplier for detecting a phase difference between a reception digital TV signal

In1 in which an interference wave signal component is included and a signal PLLout that is locked to an interference wave signal by the DPLL circuit. Reference numeral 22 denotes a data separating section for separating from each other a real component and an imaginary component of phase data that is detected by the multiplication. The separated real component Re is absorbed by a terminator 23.

The imaginary component Im separated by the data separating section 22 is supplied to a second-order loop filter 24, which has two amplifiers 24a and 24b. The gains of the first amplifier 24a and the second amplifier 24b are set at $2 \cdot Damp \cdot \omega_{n1}$ and $\omega_{n1} \cdot \omega_{n1}$, respectively, where Damp is a damping factor (usually, 0.7) of the second-order PLL circuit and ω_{n1} is a natural angular frequency of the second-order PLL circuit. An output of the second amplifier 24b is integrated by an integration circuit that consists of an adder 24d and a one-clock delay section 24e.

An output of the loop filter 24 is supplied to a modulo calculation section 25 having a period of 2π. Consisting of an adder 25a, a calculation section 25b for calculating rem(u[1]2π), and a unit delay section 25c, the modulo calculation section 25 converts input phase data into phase data (upper limit value: 2π). (For example, $2n\pi + \theta = \theta$ where n is an integer.) The phase data θ is delayed by one clock by the unit delay section 26 and then supplied to a complex exponential section (hereinafter referred to as "sinusoidal information data generation section)

27 for producing data that indicates the amplitude and the phase of the signal in the form of a complex number ($e^{j\theta}$). The sinusoidal information data generation section 27 converts the input phase data θ into data that is a complex number $r \cdot e^{j\theta} = r(\cos\theta + j \sin\theta)$ on the unit circle ($r = 1$). The sinusoidal information data generation section 27 supplies the resulting data to a conjugate signal generation section 28 for producing conjugate data $r(\cos\theta - j \sin\theta)$. An output of the conjugate signal generation section 28 is supplied to the multiplier 21 (phase comparator) as the other input signal.

In general, a clock signal of the downstream digital signal processing section can be used as a clock signal for the calculation in the phase locking section of Fig. 5. It is preferable that the clock signal of the phase locking section be synchronized with a sampling signal to be used for converting a reception IF signal into a digital signal. For example, the period of the master clock signal of the DPLL circuit is the same as the sampling period of FFT (fast Fourier transform) on a desired wave digital signal obtained by sampling at a frequency that is two times the IF frequency of a reception signal or by down-sampling. A frequency and a phase can be set by referring to a table. A PLL output is obtained that is locked to the phase of an interference wave signal having a relatively high level that is mixed in the reception digital information. More specifically, in a state that the DPLL circuit is locked to an interference wave signal,

the phase data that is output from the multiplier 21 consists of only a real component. Feedback is so performed that this real component becomes 0 next time, whereby control is so made that input complex sampling data that will act as an interference wave component in the reception channel coincides, in phase, with complex data that is output from the conjugate signal generation section 28. Therefore, in the case of the phase locking section 14a, a PLL output signal that is phase-locked to a video carrier that will act as a disturbance wave is output from the conjugate signal generation section 28 as a signal PLLout. A signal that is phase-conjugate to the phase-locked signal is output from the sinusoidal information generation section 27 as a signal ConjPLLout.

The locking range of the DPLL circuit is set in accordance with a transfer characteristic Tr of the second-order loop filter 24 and particularly depends on the total gain of the DPLL circuit. The capturing range can be determined in connection with the total gain of the PLL circuit and the time constant of the loop filter 24. The loop filter 24 is a circuit that is equivalent to a lag/lead filter as commonly used in DPLL circuits. In the case of the DPLL circuit 14a for attaining locking to a video carrier, the response speed of the loop filter 24 is set relatively low. In the case of the DPLL circuit 15a for attaining locking to an audio subcarrier, the response speed of the loop filter 24 is set high to allow it to follow a frequency shift of the

audio subcarrier because the audio subcarrier is frequency-modulated. The initial value of the DPLL circuit is set close to the frequency of an interference wave. With the channel center frequency regarded as 0, it is preferable to set the initial frequency at about -1.4652 (Freq) in the case of the phase locking section 14a for attaining locking to a video carrier and at about 1.9 (Freq2) in the case of the phase locking section 15a for attaining locking to an audio subcarrier.

As described above, in the phase locking section according to this embodiment, the DPLL circuit performs locking when the peak level of an analog video signal that is mixed in a digital TV channel is relatively high. On the other hand, in reducing interference in the same channel, the DPLL circuit does not perform locking when digital data corresponding to a disturbance frequency is not mixed in the bandwidth of a reception channel. In this case, it is preferable to output an unlock signal to the digital signal processing section and turn off the interference reducing routine. The phase locking section of Fig. 5 can also be applied to the digital receiver of Fig. 3.

Fig. 6 is a block diagram showing a specific example of the first level adjusting section 14b or the second level adjusting section 15b shown in Fig. 4. The level adjusting actions of the level adjusting sections 14b and 15b are essentially the same. Even when the amplitude of a carrier that will act as an interference wave is varied due to amplitude modulation, fading,

or the like, the level adjusting section 14b or 15b detects its variation component and outputs a level-adjusted compensation signal. The level adjusting section 14b, to which a signal that is locked to an analog video carrier that will act as an interference wave is input, compensates for a level variation that is influenced by a video modulation wave signal. The level adjusting section 15b, to which a signal that is locked to an audio subcarrier that will act as an interference wave is input, outputs a compensation signal for compensating for a relatively small level variation particularly due to fading or the like.

As shown in Fig. 6, to serve as the first level adjusting section 14b, the level adjusting section is provided with an adder 31 that receives, as an input In1, a reception digital information signal and also receives an output Lv1 of a level-compensated interference wave signal that is output from the level adjusting section 14b itself, whereby a difference component of the two signals is detected. The level adjusting section is also provided with a multiplier 32 that receives an output of the adder 31 and also receives, as an input In3, an output CPL1 that is locked by the DPLL circuit as the above-described phase locking section 14a, whereby an error signal corresponding to a level difference between the two signals is output.

Reference numeral 33 denotes a data separating section for separating data of a calculation result of the multiplier

32 into a real component and an imaginary component. The separated imaginary component Im is supplied to and absorbed by a terminator 34. The separated real component Re is supplied to a loop filter 35. The loop filter 35, which is a first-order loop filter to which the real component of the output of the multiplier 32 is supplied as an error signal, consists of an amplifier 35a for amplifying a signal at a prescribed gain, an adder 35b for integrating an output of the amplifier 35a, and a unit delay section 35c. The gain of the amplifier 35b is so set as to correspond to the reciprocal (INV TIME) of a time constant τ of the first-order loop filter 35.

An output (discrete data) of the loop filter 35 is delayed by one calculation period by a unit delay section 36 and is given "0" as an imaginary component by a data shaping section 37. The data shaping section 37 is used to provide a complex loop error signal because complex numbers are multiplied by each other in a multiplier 39. The data shaping section 37 may be omitted depending on the configuration of the multiplier 39. Receiving, as the other input In2, complex output data PLL1 or PLL2 that is locked by the above-described DPLL circuit, the multiplier 39 multiplies it by the complex loop error signal. An output of the multiplier 39 is made the other input of the adder 31.

If the level adjusting section 14b or 15b performs numerical calculation using a clock signal that is synchronized with a sampling clock signal that is used in A/D-converting reception

digital information, it becomes an AGC circuit that adjusts the output level of the DPLL circuit using the interference wave signal level as a target value. That is, where the level adjusting section is used for eliminating a video carrier as an interference wave, it compensates the level of a replica of the video carrier that is locked by the phase locking section 14a. Where the level adjusting section is used for eliminating an audio subcarrier as an interference wave, it compensates the level of a replica of the audio subcarrier that is locked by the phase locking section 15a. The level adjusting section can be used as either of the level adjusting sections 14b and 15b by changing the response characteristic of the loop filter 35 slightly. For example, the amplifier gain is set at about 0.01 (INV TIME1) for use as the level adjusting section 14b and at about 0.02 (INV TIME2) for use as the level adjusting section 15b.

For example, where the level adjusting section is used as the level adjusting section 14b, digital data In1 including an interference wave is supplied to the positive-phase input terminal of the adder 31 and data Lv1 corresponding to the level of the interference wave is supplied to its opposite-phase input terminal. Therefore, digital TV data in which the level of the interference wave corresponding to a video carrier is eliminated is output from the adder 31. On the other hand, where the level adjusting section is used as the level adjusting section 15b, a signal CompLv1 in which a video carrier interference wave is

eliminated is supplied to the positive-phase input terminal of the adder 31 and a signal corresponding to the level of the interference wave component corresponding to an audio subcarrier is supplied to its opposite-phase input terminal. Digital TV data in which the level of the interference wave corresponding to the audio subcarrier is eliminated is output from the adder 31. The digital TV data in which the level of the interference wave is eliminated and data having the carrier frequency and extracted by the above-described phase locking section 14a or 15a are supplied to the multiplier 32, and an error signal corresponding to the difference between the levels of the two signals at the carrier frequency is output from the multiplier 32.

The signal component that is output from the multiplier 32 as the error signal in this manner is input to the data separating section 33, where a real component and an imaginary component are separated from each other. The imaginary component is supplied to and absorbed by the terminator 34, and only the real component representing the level difference is supplied to the loop filter 35. The loop filter 35 is composed of a time constant circuit for attenuating a higher-frequency component and an integration circuit and has a prescribed response characteristic. An output signal of the loop filter 35 is delayed by a time corresponding to one sample data by the unit delay section 36 so as to proceed the discrete data processing and is given "0"

from a data section 38 as an imaginary component by the data shaping section 37 for complex calculation in the multiplier 39.

The multiplier 39 multiplies the error signal component that is supplied in the form of a complex number by an output signal (In2) of the DPLL circuit that is locked to the carrier that is extracted as the interference wave, whereby the level of resulting multiplication data is adjusted so as to become close to the level of the reception interference wave signal. Therefore, by subtracting the output of the multiplier 39 from the level of the interference wave signal being input to the adder 31, feedback control is so made that the real component of the error signal becomes 0. In a steady state, in this level adjusting section, the error signal component representing the level difference converges to 0. As a result, digital TV data CompLv1 or ComLv2 in which the interference wave corresponding to the video carrier or audio subcarrier is eliminated is output from the adder 31.

The level adjusting section is a digital data processing type DPLL circuit that performs known operation of an AM detector using a DPLL circuit. If a video carrier component that is input to the multiplier 32 is written as $A \cdot \cos(\omega t + \phi)$ and a carrier signal component that is phase-locked by the PLL circuit and input to the multiplier 32 is written as $K \cdot \cos\ \omega t$, a multiplication output Vo is given by $Vo = (A \cdot K/2)\cos(2\omega t + \phi) + (A \cdot K/2)\cos\phi$.

Eliminating the AC component (first term) from this equation and assuming $\phi = 0$, we obtain $Vo = A \cdot K/2$. Since $K = 1$, a signal that is proportional to the amplitude component A of the video carrier that is the interference wave is output from the multiplier 32. This level adjusting section can also be applied to the TV broadcasting receiver of Fig. 3.

Capable of being configured by digital numerical operations by reading out a program stored in a storage means or the like, the phase locking sections 14a and 15a and the level adjusting sections 14b and 15b according to this embodiment are particularly suitable for digital TV broadcasting receivers. Further, this interference reducing function can be applied to adapters for receiving a digital TV signal that are to be used in viewing a digital TV broadcast using an analog TV receiver in a transition period to digital broadcasts.